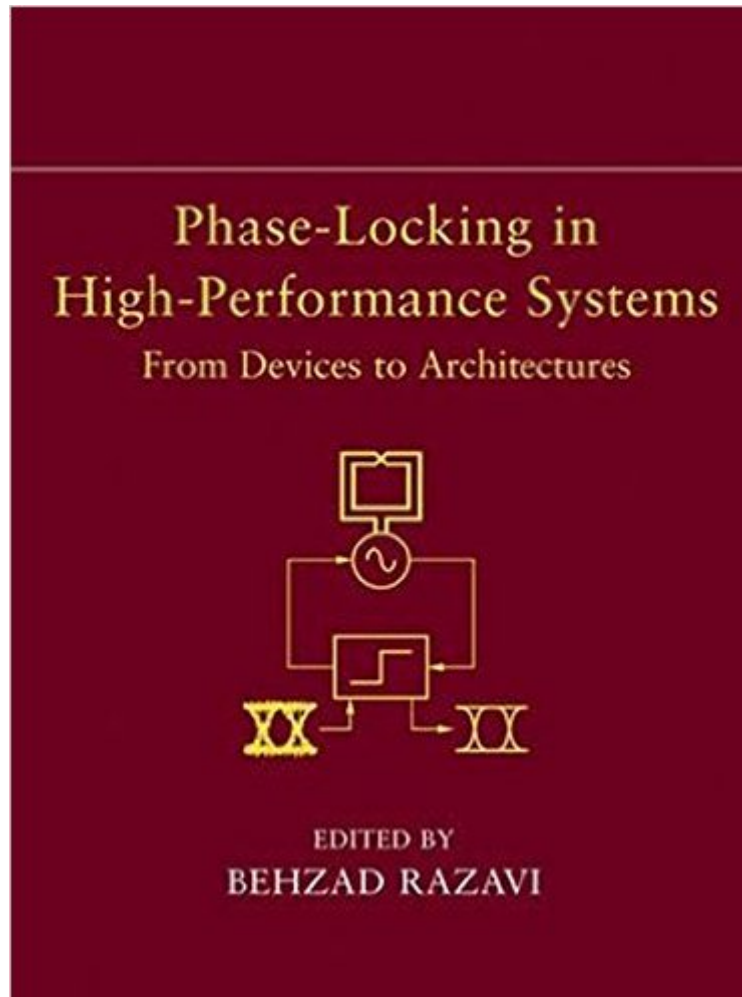


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Phase-Locking In High-Performance Systems: From Devices To Architectures



Synopsis

Comprehensive coverage of recent developments in phase-locked loop technology The rapid growth of high-speed semiconductor and communication technologies has helped make phase-locked loops (PLLs) an essential part of memories, microprocessors, radio-frequency (RF) transceivers, broadband data communication systems, and other burgeoning fields. Complementing his 1996 *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (Wiley-IEEE Press), Behzad Razavi now has collected the most important recent writing on PLL into a comprehensive, self-contained look at PLL devices, circuits, and architectures. *Phase-Locking in High-Performance Systems: From Devices to Architectures*' five original tutorials and eighty-three key papers provide an eminently readable foundation in phase-locked systems. Analog and digital circuit designers will glean a wide range of practical information from the book's . . .

- * Tutorials dealing with devices, delay-locked loops (DLLs), fractional-N synthesizers, bang-bang PLLs, and simulation of phase noise and jitter
- * In-depth discussions of passive devices such as inductors, transformers, and varactors
- * Papers on the analysis of phase noise and jitter in various types of oscillators

Concentrated examinations of building blocks, including the design of oscillators, frequency dividers, and phase/frequency detectors

- * Articles addressing the problem of clock generation by phase-locking for timing and digital applications, RF synthesis, and the application of phase-locking to clock and data recovery circuits

In tandem with its companion volume, *Phase-Locking in High-Performance Systems: From Devices to Architectures* is a superb reference for anyone working on, or seeking to better understand, this rapidly-developing and increasingly central technology.

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